WE CLAIM:

1. A voltage regulator, comprising:

an output node which is at an output voltage $V_{out}(t)$;

a linear mode voltage regulator which produces a first output voltage $V_{ol}(t)$ when activated in response to an input signal $V_i(t)$;

a high pass filter circuit connected in series between $V_{ol}(t)$ and said output node and arranged to reduce the low frequency AC and DC currents provided by said linear mode regulator to said output node to substantially zero;

a switch mode voltage regulator which produces a second output voltage $V_{osw}(t)$ when activated in response to an input signal $V_i(t)$; and

a low pass filter circuit connected in series between $V_{osw}(t)$ and said output node and arranged to isolate high frequency AC current produced by said linear mode regulator from said switch mode regulator;

such that, when activated, said linear mode regulator provides predominately high frequency AC current to said output node and said switch mode regulator provides predominately low frequency AC and DC currents to said output node, and both of said linear and switch mode regulators provide currents to said output node over a medium frequency range between said high and low frequencies, thereby providing said output voltage $V_{out}(t)$ at said output node.

2. The voltage regulator of claim 1, wherein said high pass filter circuit is a resistor connected in parallel with a capacitor such that said high pass filter

circuit reduces the low frequency AC and DC currents provided by said linear mode regulator to said output node to substantially zero.

3. The voltage regulator of claim 1, wherein said low pass filter circuit is an inductor.

4. The voltage regulator of claim 1, wherein said switch mode regulator is activated to produce $V_{osw}(t)$ in response to $V_i(t)$.

5. The voltage regulator of claim 4, wherein said switch mode regulator receives $V_i(t)$ at a first input and a signal representative of $V_{out}(t)$ at a second input and is arranged such that $V_{osw}(t)$ varies such that the difference between said first and second inputs is reduced to approximately zero.

6. The voltage regulator of claim 5, further comprising a compensation network connected between $V_{osw}(t)$ and said switch mode regulator's second input, a compensation network connected between said second input and signal ground, or both of them, to ensure the stability of said switch mode regulator.

7. The voltage regulator of claim 1, wherein $V_i(t)$ is representative of a desired $V_{out}(t)$ value.

8. The voltage regulator of claim 1, further comprising a control circuit arranged to activate said linear mode regulator and said switch mode regulator simultaneously such that a load connected to said output node is driven by both regulators.

9. The voltage regulator of claim 8, wherein said

control circuit may generate equal or different voltages for activating said linear mode and switch mode regulators such that a load connected to said output node is driven by both regulators.

10. The voltage regulator of claim 8, wherein said linear mode regulator has a faster response speed than said switch mode regulator such that said linear mode regulator contributes the majority of the high frequency AC current to said load and said switch mode regulator contributes the majority of the low frequency AC and DC output currents to said load.

11. The voltage regulator of claim 1, wherein said load is at least one or more laser diodes.

12. The voltage regulator of claim 1, wherein said high pass filter circuit comprises a resistor and a capacitor connected in parallel such that said capacitor conducts high frequency AC current to said output node and said resistor reduces the low frequency AC and DC currents provided by said linear regulator to said output node to substantially zero

13. The voltage regulator of claim 1, wherein said high pass filter circuit comprises a capacitor which conducts high and medium frequency AC currents to said output node.

14. The voltage regulator of claim 1, wherein said high pass filter circuit is a current sense resistor connected in parallel with a capacitor, and said switch mode regulator produces $V_{osw}(t)$ in response to an input signal, further comprising an operational amplifier having its inputs connected across said current sense resistor and

said capacitor, and its output connected to provide said switch mode regulator's input signal, said operational amplifier and switch mode regulator arranged to drive said output node with the low frequency AC and DC currents so that the current going through said sense resistor is nearly zero such that, during operation, said linear mode regulator provides predominately high frequency AC current to said output node and said switch mode regulator provides predominately low frequency AC and DC currents to said output node.

15. The voltage regulator of claim 1, wherein said switch mode regulator produces $V_{osw}(t)$ at an output terminal in response to $V_i(t)$, said switch mode regulator comprising:

an operational amplifier connected to produce an output which varies with the difference between its two inputs, one of which is derived from $V_{out}(t)$ and the other of which is derived from $V_i(t)$,

a comparator which receives the output of said operational amplifier at a first input and a sawtooth-shaped clock signal at its second input, and is arranged to produce a pulse-width modulated signal at its output,

an output inductor connected between the output of said comparator and said output node, and

a capacitor connected between said output node and ground.

16. The voltage regulator of claim 15, wherein said operational amplifier receives a signal that is derived from $V_i(t)$ at one input and a signal which is derived from $V_{out}(t)$ at its second input, further comprising a compensation network connected between $V_{out}(t)$ and said operational amplifier's second input, a compensation network connected between said second input and signal ground, or having both of the two compensation network

circuits employed at the same time, to ensure and/or improve the stability of said operational amplifier.

17. A voltage regulator, comprising:

an output node which is at an output voltage $V_{out}(t)$;

a linear mode voltage regulator which receives an input signal $V_i(t)$ representative of a desired $V_{out}(t)$ value and is arranged to produce a first regulated output voltage $V_{ol}(t)$ which varies with $V_i(t)$;

a high pass filter comprising a resistor connected in parallel with a capacitor, said high pass filter connected in series between $V_{ol}(t)$ and said output node and arranged to reduce the low frequency AC and DC currents provided by said linear mode regulator to said output node to substantially zero;

a switch mode voltage regulator which receives $V_i(t)$ and is arranged to produce a second regulated output voltage $V_{osw}(t)$ which varies with $V_i(t)$; and

an inductor connected in series between $V_{osw}(t)$ and said output node which isolates the high frequency AC current produced by said linear mode regulator from being drawn by said switch mode regulator;

such that said linear mode regulator provides predominately the high frequency AC current to said output node and said switch mode regulator provides predominately the low frequency AC and DC currents to said output node, and both of said linear and switch mode regulators provide currents to said output node in a medium frequency range between said high and low frequencies, thereby providing said output voltage $V_{out}(t)$ at said output node.

18. A voltage regulator, comprising:

an output node which is at an output voltage $V_{out}(t)$;

a linear mode voltage regulator which receives an input signal $V_i(t)$ representative of a desired $V_{out}(t)$ value and is arranged to produce a first regulated output voltage $V_{ol}(t)$ which varies with $V_i(t)$;

a current sense resistor and a capacitor connected in parallel, connected in series between $V_{ol}(t)$ and said output node which allows high frequency AC current to pass through and low frequency and DC current to generate a voltage $V_{is}(t)$ across said current sense resistor and said capacitor;

an operational amplifier having its inputs connected across said parallel-connected current sense resistor and capacitor which produces an output that varies with the difference between its inputs;

a switch mode voltage regulator which receives a signal $V_{osw}(t)$ at one input and the output of said operational amplifier at a second input and which produces an output voltage $V_{osw}(t)$ that varies with the difference between its inputs; and

an inductor connected in series between $V_{osw}(t)$ and said output node $V_{out}(t)$ which isolates high frequency AC current produced by said linear mode regulator from being drawn by said switch mode regulator;

such that said operational amplifier senses the low frequency AC and DC currents going through said current sense resistor and said capacitor, drives said switch mode regulator and thereby said output node to make $V_{ol}(t) \approx V_{out}(t)$ for low frequency and DC components, such that the low frequency AC and DC currents going through said current sense resistor and said capacitor are reduced to approximately zero, so that said linear mode regulator provides predominately high frequency AC current to said output node and said switch mode regulator provides predominately low frequency AC and DC currents to said output node, thereby providing said output voltage $V_{out}(t)$

at said output node.